1. A method of fabricating a metal oxide semiconductor field effect transistor, (MOSFET), device, on a semiconductor substrate, comprising the steps of:

forming a gate structure, overlying a gate insulator layer, on said semiconductor substrate;

growing a first silicon oxide layer on said gate structure, and on the top surface of regions of said semiconductor substrate not covered by said gate structure;

performing a first ion implantation procedure to form a lightly doped source/drain, (LDD), region, in an area of said semiconductor substrate not covered by said gate structure;

depositing a second silicon oxide layer;

performing a second ion implantation procedure to create a nitrogen region at the first silicon oxide - LDD interface;

forming composite insulator spacers on the sides of said gate structure;

performing a third ion implantation procedure to form a heavily doped source/drain region in an area of said semiconductor substrate not covered by said gate structure, or by said composite insulator spacers; and

performing an anneal procedure.

2. The method of claim 1, wherein said MOSFET device is an input/output N channel, (I/O NMOS), device.

3. The method of claim 1, wherein said gate insulator layer is a silicon dioxide layer, thermally grown to a thickness between about 40 to 80 Angstroms, at a temperature between about 650 to 900° C, in an oxygen - steam ambient.

4. The method of claim 1, wherein said gate structure is a polysilicon gate structure, comprised from a polysilicon layer which is obtained via LPCVD procedures, at a thickness between about 1500 to 2500 Angstroms, and either doped in situ, during deposition, via the addition of arsine, or phosphine, to a silane ambient, or deposited intrinsically then doped via implantation of arsenic, or phosphorous ions.

5. The method of claim 1, wherein said gate structure is defined via an anisotropic RIE procedure, applied to a polysilicon layer, using Cl_2 or SF_6 as an etchant.

6. The method of claim 1, wherein said first silicon oxide layer is thermally grown to a thickness between about 15 to 80 Angstroms, at a temperature between about 800 to 1015° C, in an oxygen -steam ambient.

7. The method of claim 1, wherein said first ion implantation procedure, used to form said LDD region, is performed using arsenic or phosphorous ions, at an energy between about 20 to 50 KeV, at a dose between about 2E13 to 5E13 atoms/cm^2.

8. The method of claim 1, wherein said second silicon oxide layer, is obtained via LPCVD or PECVD procedures, at a thickness between about 80 to 250 Angstroms, using tetraethylorthosilicate, (TEOS), as a source.

9. The method of claim 1, wherein said second ion implantation procedure, used to create said nitrogen region, is performed using either nitrogen, (N_2^+), or nitrogen ions, (N^+), as a source, at an energy between about 5 to 25 KeV, at a dose between about 1E14 to 1E15 atoms/cm^2.

10. The method of claim 1, wherein said composite insulator spacers are comprised of an underlying silicon nitride layer, obtained via LPCVD or PECVD procedures, at a thickness between about 200 to 400 Angstroms, and comprised of an overlying silicon oxide layer, obtained via LPCVD or PECVD procedures, at a thickness between about 850 to 1100 Angstroms, using TEOS as a source.

11. The method of claim 1, wherein said composite insulator spacers are defined via an anisotropic RIE procedure using CHF_3 as an etchant for silicon oxide, and using Cl_2 as an etchant for silicon nitride.

12. The method of claim 1, wherein said third ion implantation procedure, used to create said heavily doped source/drain region, is performed using arsenic or phosphorous ions, at an energy between about 40 to 60 KeV, at a dose between about 3E15 to 6.5E15 atoms/cm^2.

13. The method of claim 1, wherein said anneal procedure is a rapid thermal anneal, (RTA), procedure, performed at a temperature between about 1000 to 1050° C, for a time between about 5 to 15 sec, in a nitrogen or argon ambient.

14. A method of fabricating an input/output N channel, (I/O NMOS), device, on a semiconductor substrate, featuring an implanted nitrogen region, located at an interface of an overlying insulator layer and an underlying, lightly doped source/drain, (LDD), region, comprising the steps of:

growing a silicon dioxide gate insulator layer on said semiconductor substrate;

forming a polysilicon gate structure on said silicon dioxide gate insulator layer;

growing a silicon oxide layer on the surface of said polysilicon gate structure, and on the surface of portions of said semiconductor substrate not covered by said polysilicon gate structure;

using tetraethylorthosilicate as a source to deposit a TEOS silicon oxide liner layer;

performing a first ion implantation procedure to form an N type LDD region in an area of said semiconductor substrate not covered by said polysilicon gate structure;

performing a second ion implantation procedure in situ, to form said nitrogen region at said silicon oxide - N type LDD interface;

forming composite insulator spacers on sides of said polysilicon gate structure, comprised of an overlying silicon oxide shape, and an underlying silicon nitride shape;

performing a third ion implantation procedure to form an N type, heavily doped source/drain region, in an area of said semiconductor substrate not covered by said polysilicon gate structure, or by said composite insulator spacers; and

performing a rapid thermal anneal, (RTA), procedure.

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15. The method of claim 14, wherein said silicon dioxide gate insulator layer is obtained via thermal oxidation procedures, at a temperature between about 650 to 900° C, in an oxygen - steam ambient, to a thickness between about 40 to 80 Angstroms..

16. The method of claim 14 wherein said polysilicon gate structure is comprised from a polysilicon layer, which is obtained via LPCVD procedures, at a thickness between about 1500 to 2500 Angstroms, and either doped in situ, during deposition via the addition of arsine, or phosphine, to a silane ambient, or deposited intrinsically the doped via implantation of arsenic, or phosphorous ions, then defined via an anisotropic RIE procedure, applied to a polysilicon layer, using Cl_2 or SF_6 as an etchant.

17. The method of claim 14, wherein said silicon oxide layer is obtained via thermal oxidation procedures, at a temperature between about 800 to 1015° C, in an oxygen - steam ambient, to a thickness between about 15 to 80 Angstroms.

18. The method of claim 14, wherein said TEOS silicon oxide liner layer is deposited to a thickness between about 80 to 250 Angstroms, via LPCVD or PECVD procedures, using tetraethylorthosilicate, (TEOS), as a source.

19. The method of claim 14, wherein said first ion implantation procedure, used to form said N type LDD region, is performed using arsenic or phosphorous ions, at an energy between about 20 to 50 KeV, at a dose between about 2E13 to 5E13 atoms/cm^2.

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20. The method of claim 14, wherein said second ion implantation procedure, used to create said nitrogen region, is performed using either nitrogen, (N_2^+), or nitrogen ions, (N+), as a source, at an energy between about 5 to 25 KeV, at a dose between about 1E14 to 1E15 atoms/cm^2.

21. The method of claim 14, wherein said composite insulator spacers are comprised of an underlying silicon nitride layer, obtained via LPCVD or PECVD procedures, at a thickness between about 200 to 400 Angstroms, and comprised of an overlying silicon oxide layer, obtained via LPCVD or PECVD procedures, at a thickness between about 850 to 1100 Angstroms, using TEOS as a source.

22. The method of claim 14, wherein said third ion implantation procedure, used to create said N type, heavily doped source/drain region, is performed using arsenic or phosphorous ions, at an energy between about 40 to 60 KeV, at a dose between about 3E15 to 6.5E15 atoms/cm^2.

23. The method of claim 14, wherein said rapid thermal anneal procedure is performed at a temperature between about 1000 to 1050° C, for a time between about 5 to 15 sec, in a nitrogen or argon ambient.

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